METHODS AND SYSTEMS FOR DETECTING DEFECTS IN SERIAL LINK TRANSCEIVERS

Inventor: Pieter Vorenkamp

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/516,735, titled, "Methods and Systems for Detecting Defects in Serial Link Transceivers," filed November 4, 2003, incorporated herein by reference in its entirety.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention is directed to serial link transceivers and, more particularly, to detecting defects in serial link transceivers.

Related Art

[0003] Serial link transceivers, including but not limited to differential AC-coupled high-speed links, are susceptible to defects such as manufacturing defects. Such defects can include shorts between transmission lines and ground, shorts between transmission lines and power supplies, and open circuits in transmission lines.

[0004] There is thus a need for methods and systems for detecting defects in serial link transceivers.

SUMMARY OF THE INVENTION

[0005] The present invention is directed to methods and systems for detecting defects in serial link transceivers. The invention can be implemented in, for example and without limitation, an AC-coupled differential high-speed serial link transceiver ("transceiver"). In such a transceiver, a transmitter and receiver are coupled through differential AC-coupled or DC-coupled

transmission lines, and the receiver can include a common mode control circuit. In accordance with the invention, a monitoring system detects one of:

[0006] open circuits in one of the transmission lines;

[0007] short circuits between one or more of the transmission lines and a power supply or ground plane;

[0008] short circuits between the transmission lines; and

[0009] short circuits across the AC-coupling capacitors.

[0010] Additional features and advantages of the invention will be set forth in the description that follows. Yet further features and advantages will be apparent to a person skilled in the art based on the description set forth herein or may be learned by practice of the invention. The advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0011] It is to be understood that both the foregoing summary and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS/FIGURES

[0012] The present invention will be described with reference to the accompanying drawings, wherein like reference numbers indicate identical or functionally similar elements. Also, the leftmost digit(s) of the reference numbers identify the drawings in which the associated elements are first introduced.

[0013] FIG. 1 is a block diagram of an example differential serial-link transceiver ("transceiver") 100.

[0014] FIG. 2 is a block diagram of the transceiver 100, wherein a variety of potential defects are represented as shorts and/or open circuits.

[0015] FIG. 3 is a block diagram of the differential receiver 104, including a common-mode control circuit Vcm 302.

[0016] FIG. 4 is a block diagram of the receiver 104, including an example monitoring system 402.

[0017] FIG. 5 is a flowchart of a method for detecting defects in a serial link transceiver.

[0018] FIG. 6 is a flowchart of step 504 from FIG. 5.

DETAILED DESCRIPTION OF THE INVENTION

Introduction

[0019] FIG. 1 is a block diagram of an example differential serial-link transceiver ("transceiver") 100. The transceiver 100 includes a differential transmitter 102, a differential receiver 104, and a differential link 106. The differential link 106 includes differential transmission line 108 and 110. The differential transmitter 102 outputs Vp on the one leg of the differential transmission line 108, and Vn on the other leg of the differential transmission line 110. In the example of FIG. 1, the transmitter 102 and receiver 104 are AC coupled through capacitors 112 and 114, respectively. Alternatively, the capacitors 112 and 114 are omitted and the transmitter 102 and receiver 104 are DC coupled.

Defect Detection

[0020] The differential transceiver 100, or portions thereof, are typically implemented on one or more printed circuit boards ("PCBs"). Defects in the PCBs can be encountered during manufacturing and/or subsequent handling. Defects in the PCBs can reduce the performance of the transceiver 100 and/or render the differential transceiver 100 inoperable.

[0021] FIG. 2 is a block diagram of the transceiver 100, wherein a variety of potential defects are represented as shorts and/or open circuits. The potential defects are described below.

[0022] The present invention is directed to methods and systems for detecting one of the defects represented in FIG. 2. Systems for detecting one of the defects represented in FIG. 2 include a monitoring circuit such as, without limitation, a voltage and/or current monitoring circuit.

[0023] The monitoring circuit can be implemented to directly or indirectly detect a defect. A direct monitoring circuit can be coupled to either of the

differential transmission lines 108 and 110. An indirect monitoring circuit can be coupled to a circuit that supports the transceiver 100. For example, and without limitation, an indirect monitoring circuit can be coupled to a common mode control circuit that supports the transceiver 100. An indirect monitoring circuit has the advantage of not adding additional high speed circuitry to the transmission lines, and thus does not degrade system performance.

[0024] FIG. 3 is a block diagram of a differential receiver 104, including an example common-mode control circuit Vcm 302. The common-mode control circuit maintains signals on the transmission lines 108 and 110 centered about a common mode voltage. Common-mode control circuits are well known in the art.

[0025] Under normal operating conditions, the common-mode control circuit Vcm 302 provides substantially zero DC current and zero AC current to the differential transmission lines 108 and 110. When there is a defect in the differential transceiver 100, however, the common-mode control circuit Vcm 302 will provide a DC current and/or an AC current to transmission line 108 and/or to transmission line 110 to maintain signal levels thereon at desired common mode levels.

[0026] Referring back to FIG. 2, example potential defects and corresponding reactions of the common-mode control circuit Vcm 302 are now described. The invention is not, however, limited to transceivers that include common-mode control circuits. The invention is also not limited to AC-coupled transceivers.

[0027] The example potential defects include fourteen potential defects in the positive and negative signal lanes (i.e., transmission lines 108 and 110). The potential defects also include two potential shorts between the positive and negative signal lanes, and two potential cross shorts across the AC coupling capacitances 112 and 114. The example potential defects are now described in detail with reference to FIG. 2.

[0028] R1p represents a potential open circuit in the transmission line 108 between the transmitter 102 and the capacitor 112. When this occurs, the

common-mode control circuit Vcm 302 provides an AC current that tracks Vin in an attempt to maintain signals on the transmission lines at a common mode voltage.

[0029] R2p represents a potential short between the transmission line 108 and a power supply VDD between the transmitter 102 and the capacitor 112. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vp.

[0030] R3p represents a potential short between the transmission line 108 and a power supply VSS between the transmitter 102 and the capacitor 112. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vp.

[0031] R4p represents a potential short across the capacitor 112. When this occurs, the common-mode control circuit Vcm 302 sinks or sources a DC current.

[0032] R5p represents a potential short between the transmission line 108 and the power supply VDD between the capacitor 112 and the receiver 104. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vp.

[0033] R6p represents a potential short between the transmission line 108 and the power supply VSS between the capacitor 112 and the receiver 104. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vp.

[0034] R7p represents a potential open in the transmission line 108 between the capacitor 112 and the receiver 104. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vp.

[0035] R1n represents a potential open in the transmission line 110 between the transmitter 102 and the capacitor 114. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vn.

[0036] R2n represents a potential short between the transmission line 110 and the power supply VDD between the transmitter 102 and the capacitor 114.

When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vn.

[0037] R3n represents a potential short between the transmission line 110 and the power supply VSS between the transmitter 102 and the capacitor 114. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vn.

[0038] R4n represents a potential short across the capacitor 114. When this occurs, the common-mode control circuit Vcm 302 sinks or sources a DC current.

[0039] R5n represents a potential short between the transmission line 110 and the power supply VDD between the capacitor 114 and the receiver 104. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vn.

[0040] R6n represents a potential short between the transmission line 110 and the power supply VSS between the capacitor 114 and the receiver 104. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vn.

[0041] R7n represents a potential open circuit in the transmission line 110, between the capacitor 114 and the receiver 104. When this occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vn.

[0042] R1d and R2d represent potential shorts between the transmissions line 108 and 110. When R1d or R2d occurs, no signal is presented at the receiver 104.

[0043] R1x and R2x represent potential shorts or cross-faults across the AC coupling capacitances 112 and 114. When R1x occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vn. When R2x occurs, the common-mode control circuit Vcm 302 provides an AC current that tracks Vp.

[0044] Defects in the differential transceiver 100 can reduce the performance of the differential transceiver 100 and/or render it inoperable. Therefore, it is useful to know when there is a defect in the differential transceiver 100.

[0045] In many situations, it is sufficient to know that there is a defect in the differential transceiver 100. It is often not necessary to know the precise location of the defect, the precise nature of the defect, or the precise number of defects. For example, IEEE 1149.1 is an IEEE supported standard directed to detecting PCB manufacturability issues using on-chip monitoring functions. IEEE 1149.6 is an extension to the IEEE1149.1 standard directed to high-speed differential signal lines using AC-coupling, such as in serializer/deserializer ("SERDES") transceivers. IEEE 1149.6 stipulates that defects be detectable using a pass/fail criteria. IEEE 1149 is incorporated herein by reference in its entirety.

[0046] Accordingly, the present invention is directed to methods and systems for detecting the presence of at least one serial-link interconnect defect.

[0047] Recall from above that the invention can be implemented by monitoring voltage or current, directly or indirectly. An example is provided below for indirectly monitoring current. The invention is not, however, limited to this example. Based on the description herein, one skilled in the relevant art(s) will understand how to detect a defect by monitoring voltage or current, directly or indirectly.

[0048] In the example of FIG. 3, the transceiver 100 includes a common-mode control circuit Vcm 302. In accordance with the invention, current provided by the common-mode control circuit Vcm 302 is monitored to indirectly detect one or more of the conditions discussed above. For example, AC and/or DC current provided by the common-mode control circuit Vcm 302 is monitored. When the AC and/or DC current provided by the common-mode control circuit Vcm 302 exceeds corresponding AC and/or DC current thresholds, a defect is declared. For AC and/or DC current monitoring, the corresponding threshold can be a fixed level. Alternatively, or additionally, the AC threshold is dynamically determined relative to Vp and/or Vn, and/or relative to one or more other variables.

[0049] Based on the description herein, one skilled in the relevant art(s) will understand that any conventional and/or yet to be developed current and/or

voltage monitoring methods and/or systems, and/or combinations thereof, can be employed.

[0050] FIG. 4 is a block diagram of the receiver 104, including an example monitoring system 402. In the example of FIG. 4, the monitoring system 402 is configured to monitor AC and/or DC current and/or voltage that is provided by the common-mode control circuit Vcm 302. Current and voltage monitoring systems are well known in the art.

[0051] In the example of FIG. 4, the monitoring system 402 is an indirect monitoring system. In alternative embodiments, the monitoring system 402 is coupled directly to one of the differential transmission lines 108 or 110 to monitor current or voltage directly.

[0052] The monitoring system 402 includes one or more of a variety of conventional and/or yet to be developed current monitoring systems, methods, and/or combinations thereof.

[0053] The monitoring system 402 includes one or more outputs 404 for outputting results of the monitoring. The monitoring system 402 outputs a fault indication on the output(s) 404 when the monitoring system 402 senses one or one or more current conditions indicative of the potential defects described herein.

[0054] In the example of FIG. 4, the monitoring system 402 is coupled between the common-mode control circuit Vcm 302 and a common-mode control circuit resistance Rcm 304. Alternatively, the monitoring system 402 is coupled between the common-mode control circuit resistance Rcm 304 and the transmission lines 108 and 110. Alternatively, the monitoring system 402 is coupled to a node between the common-mode control circuit Vcm 302 and the common-mode control circuit resistance Rcm 304, or to a node between the common-mode control circuit resistance Rcm 304 and the transmission lines 108 and 110, so that the monitoring system 402 is not directly in the Vcm signal path. Thus, when the monitoring system 402 is implemented as an indirect monitoring system, the invention does not require additional high-

speed circuitry in the transmission lines 108 and/or 110, and thus does not degrade dynamic performance of the differential transceiver 100.

[0055] Alternatively, the monitoring system 402 is coupled directly to the transmission line 108 and/or 110.

[0056] FIG. 5 is a flowchart of a method 500 for indirectly detecting defects in a serial link transceiver having a common-mode control circuit, as illustrated in FIGS. 3 and 4. The method 500 is described in terms of monitoring current from a common-mode control circuit Vcm. The invention is not, however, limited to indirectly detecting defects and/or to current monitoring. Based on the disclosure herein, one skilled in the relevant art(s) will understand how to implement the invention to directly detects, and how to implement the invention to detect defects based on voltage monitoring, with and without a common-mode control circuit.

[0057] The method illustrated in the flowchart of FIG. 5 can be implemented with circuitry described above, and/or with any other suitable circuitry. The process begins at step 502, which includes sensing an output of the common-mode control circuit Vcm, without adversely affecting data transmission (e.g., without degrading dynamic performance of the transceiver).

[0058] Step 504 includes outputting an indication of a defect when the sensed output of the common-mode control circuit Vcm exceeds a threshold. Step 504 can be implemented to detect one or more of the potential defects described above. For example, FIG. 6 illustrates step 504 implemented with steps 602-608.

[0059] Step 602 includes outputting an indication of a defect when AC output of the common-mode control circuit Vcm tracks Vin. Step 602 is useful, for example, for detecting open circuits in the transmission line 108 and shorts between the transmission line 108 and a power supply. Step 602 is useful in other situations as well, as will be apparent to one skilled in the relevant art(s) after reading the description herein.

[0060] Step 604 includes outputting an indication of a defect when AC output from the common-mode control circuit Vcm tracks Vip. Step 604 is useful for

detecting open circuits in the inverted transmission line 110 and shorts between the inverted transmission line 110 and a power supply.

[0061] Step 606 includes outputting an indication of a defect when no signal is presented at the receiver and a current and/or voltage output is provided by common-mode control circuit Vcm. Step 606 is useful for detecting short circuits between the transmission lines.

[0062] Step 608 includes outputting an indication of a defect when a DC output is provided by common-mode control circuit Vcm. Step 608 is useful for detecting short circuits across AC couplings.

Conclusion

[0063] The present invention has been described above with the aid of functional building blocks illustrating the performance of specified functions and relationships thereof. The boundaries of these functional building blocks have been arbitrarily defined herein for the convenience of the description. Alternate boundaries can be defined so long as the specified functions and relationships thereof are appropriately performed. Any such alternate boundaries are thus within the scope and spirit of the claimed invention. One skilled in the art will recognize that these functional building blocks can be implemented by discrete components, application specific integrated circuits, processors executing appropriate software and the like and combinations thereof.

[0064] While various embodiments of the present invention have been described above, it should be understood that they have been presented by way of example only, and not limitation. Thus, the breadth and scope of the present invention should not be limited by any of the above-described exemplary embodiments, but should be defined only in accordance with the following claims and their equivalents.